Jerry T. Healey

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Professional Experience:

President - Threshold Systems 2007 - present
1998 - 2004

- Manage a consulting firm which specializes in:
  - short course technology instruction for engineers and scientists regarding state-of-the-art Process Integration, Semiconductor Fabrication down to the 5nm node and Device-Process interactions
  - clients include KLA-Tencor, Qualcomm, Air Liquide, Versum, Dow Chemical, JXP Nippon, Motorola, Aligent, ASML, Nova Measuring Instruments, Toyko Electron, Applied Materials, LAM Research and many others.
  - technical consulting for client companies regarding Technology Road Maps, identifying research and development opportunities, and preparing research reports on emerging technologies
  - provide advice and resolution strategies to manufacturers on process integration issues and yield optimization for Logic
  - qualification of semiconductor fabrication facilities for clients as well as yield crisis resolution and the creation of Technology Roadmaps
  - expert witness for litigation involving semiconductor processing and IP issues

Expert Witness *April 2008* - Oct. 2009

- Acted as the lead expert witness in a multi-billion-dollar litigation between two major Asian semiconductor manufacturers
- Conducted a detailed analysis of four generations of process flows to ascertain the veracity of trade secret claims
- Examined in excess of 1,000 papers and patents in a prior art search to establish that certain trade secret claims were publicly available and/or readily ascertainable. Wrote a detailed report on the results of this research.
- Testified in an eight-hour deposition as well as well as took the stand for three hours in Federal court in Alameda County California, to opine on the validity of specific trade secret claims

Baseline Integration Engineer
Sematech's **Advanced Technology Development Center (ATDF)** April 2004 – Jan. 2006

- Managed a 90 nm research baseline and was responsible for leading teams of engineers to resolve all technical issues associated with this process flow and for maintaining the line stability
- Resolved processing issues on a leading-edge high-k/metal gate logic process flow
- Acted as the key development engineer on the ATDF 45 nm development effort, assuming responsibility for engineering the transistor gate stack
- Interfaced with Front End Process R&D on a daily basis and addressed their fabrication concerns, as well as integrated their new process modules into the baseline process

Instructor - UC Berkeley Extension, College of Engineering 1995 – 2004
University of California at Berkeley, Berkeley, California

- A key lecturer for UC Berkeley's public courses on the subjects of Process Integration for the highly acclaimed courses: "Silicon processing for the VLSI Era", "Process Integration for Sub-Micron Technologies"

Senior Process Integration Engineer
Motorola Semiconductor, Austin, Texas. 1994 - 1998

- Orchestrated the transfer of a range of high-performance Logic parts featuring embedded Non-Volatile and embedded DRAM memory elements from Motorola's research facility (APRDL) into a manufacturing environment, and solved numerous process integration problems associated with these devices
- Made numerous presentations to senior management and Design and Process Engineering staffs, as well as directly to customers

Technology Transfer Device Engineer **- Advanced Microcontrollers**

Motorola Semiconductor, Austin, Texas. 1993 - 1994

- Successfully transferred numerous 16/32-bit microcontrollers and other complex multi-function Logic devices from R&D into high-volume production, and systematically enhanced their yields
- Interfaced with Design, Test, Product Engineering, and Manufacturing, and lead cross-functional groups to resolve technical problems associated with the manufacture of state-of-the-art ICs

Device Engineer

Motorola Semiconductor, Austin, Texas. 1991 - 1993

- Managed the production of a large portfolio of digital/analog Logic devices for Custom Automotive, Telecom, and Advanced Microcontroller Systems
- Designed experiments to isolate and identify the sources of yield loss and conducted failure analysis to successively enhance the yield of these devices

Education:

Master of Science - Semiconductor Physics Graduated 1990
University of Utah, Salt Lake City, Utah.

Bachelor of Science - Science Graduated 1984
University of Waterloo, Waterloo Ontario, Canada.

Special Skills:

- Excellent communication skills - written and verbal
- Outstanding people skills

Activities:

- Technical rock climbing, technical ice climbing, rowing, bicycling, canyoneering

Publications:

Papers

- Jerry Healey & Craig Franklin**, "The Prevention of Polyimide Stringers on Bonding Pads",** *Interface '93 Microlithography Seminar Proceedings*; September 1993.

- Jerry Healey & George Kong**,"The Reduction of Low-Level Current Leakage in CMOS Devices"**, *Microelectronics Manufacturability, Yield, and Reliability*, October 1994.

- Jerry Healey, Tony Phan & Randy Kent**,"The Prevention of Auto Doping induced Threshold Voltage Shifts"**, *SPIE The International Society for optical Engineering*, October 1, 1995.

- Jerry Healey & Tony Phan **,"The Role of RIE in Microchip Bond Pad Corrosion";** *SPIE The International Society for optical Engineering*, October 16, 1996.

- Jerry Healey & Neil Henis**,"Yield Enhancement Through Monitoring of Real Time Manufacturing Processes"**, *Future Fab International*, January 1, 1997.

- Jerry Healey & Scott Rubel **,"The Influence of Topographical Variations on Reliable Via and Contact Formation",** *Microelectronics Manufacturability, Yield, and Reliability*, August 1999.

- Jerry Healey, "**Dual Damascene and Low-K Dielectrics",** web publication, www.siliconnexus.com, 2002. (17,000 copies downloaded).

Books:

- Jerry Healey "**Advanced CMOS Technology – The 10nm Node**", Sixth Edition, *Ricoh Publications*, 590 pages, June, 2016.

- Jerry Healey, "**Advanced CMOS Technology – The 5nm Node**", eighth Edition, *Extension Media Press*, 600 pages, April, 2018.

- Jerry Healey "**14nm FinFET Processing**", fourth edition, *Extension Media Press*, 194 pages, February, 2015.

- Jerry Healey, "**Fundamentals of Microchip Design and Fabrication**" twelfth Edition, *Taylor Communications*, 198 pages, January, 2019

- Jerry Healey "**Process Integration for Logic and Memory**", third edition, *Ricoh Publications*, 196 pages, March, 2015.

- Jerry Healey "**The Transition from 28nm to 22nm Processing**", second edition, *Ricoh Publications*, 215 pages, September, 2014.

- Jerry Healey "**22nm FinFet Processing**", second edition, *Mimeo Media*, 215 pages, October, 2014.

- Jerry Healey "**The 3D packaging Revolution**", First Edition, *Ricoh Publications*, 198 pages, March, 2017.