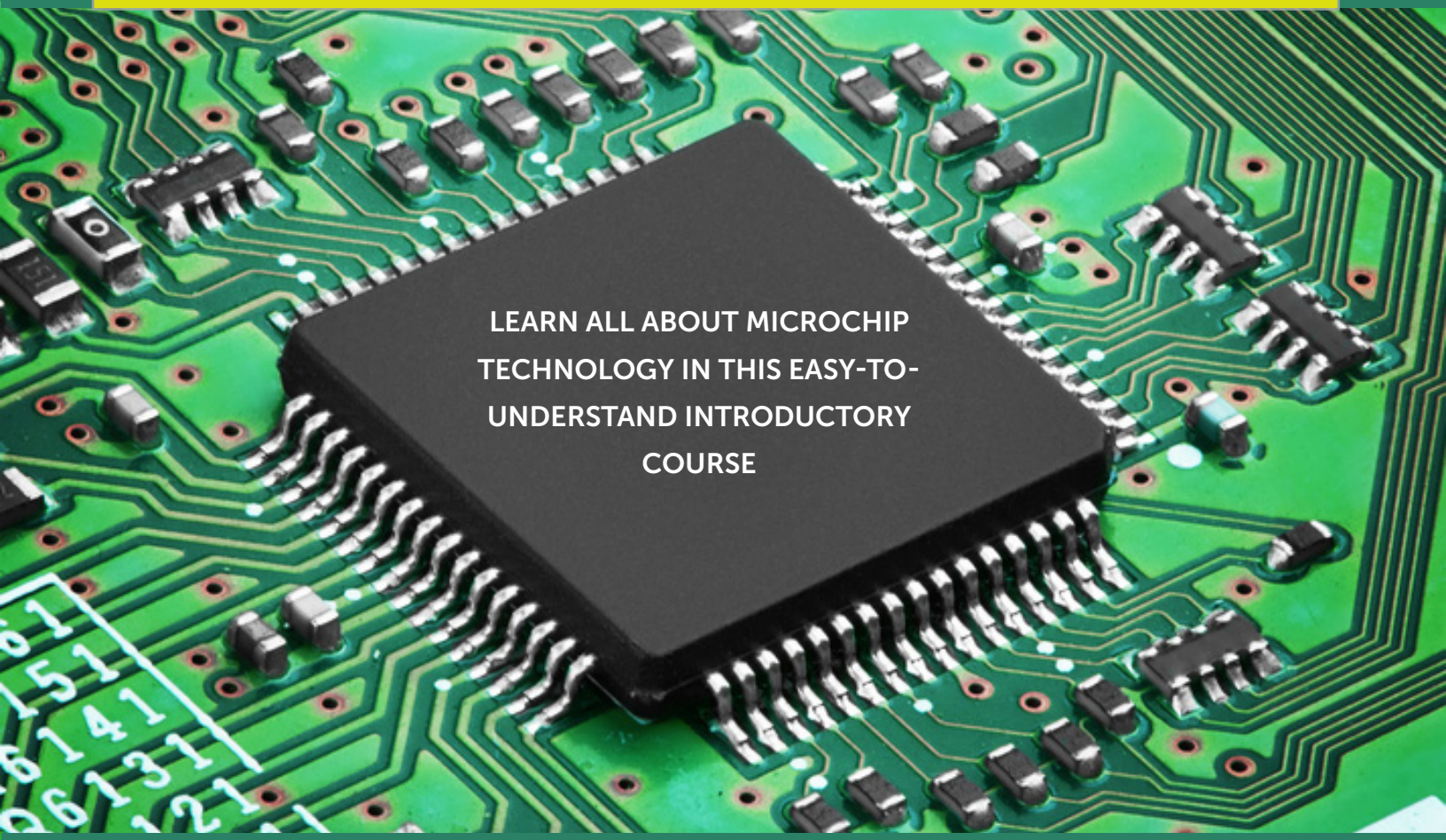
# FUNDAMENTALS OF MICROCHIP DESIGN & FABRICATION

## An ONLINE Course

*COURSE CONTENT IS UPDATED & TECHNICALLY CURRENT AS OF OCTOBER 2021*




1. Semiconductor Fundamentals: PN junctions, MOSFETs, Memory versus Logic
2. Microchip scaling; what is a technology node?
3. Microchip Design: Logic gates, physical layout, Logic design, simulation tools, chip layout, design rule checks, mask generation
4. Microchip Process technology: ALD, CMP, CVD, Electroplating, Etch, Ion implantation, Lithography, PVD, and RTP
5. Microchip Fabrication: A step-by-step fabrication sequence for a FinFET transistor and a Nanosheet transistor
6. Microchip Packaging: Chip Scale Packaging, Wafer Level Packaging, the flip-chip packaging, System-in-Package Multi-Chip Modules, System on Chip, stacked die, Package-in-Package, Package-on-Package, 3D packaging

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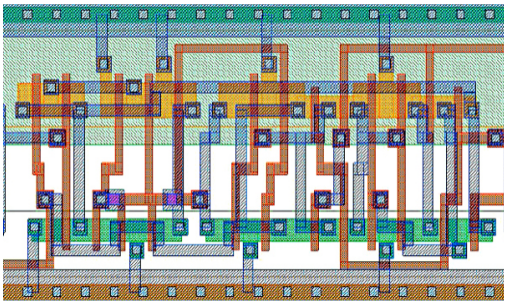
# Fundamentals of Microchip Design & Fabrication

AN ONLINE COURSE



*Are you new to the semiconductor industry, or need a refresher course on microchip fabrication technology?*
*This course provides an excellent introduction to the science of IC design and fabrication as well as an overview of microchip packaging. It is introductory in nature, explanatory in tone, and covers the most basic concepts of microchip design and manufacturing in simple, easy-to understand terms.*

## Online Learning

The Covid-19 pandemic and the travel restrictions it has imposed have changed the landscape of technical instruction from traditional instructor-lead classroom learning toward a distributed learning experience that enables the instructor and the students to be in socially distant locations. This learning solution eliminates high cost and inconvenience associated with having students travel to one location for instruction. It offers a safe, flexible, convenient and less expensive learning experience that traditional classroom instruction does not have. It is also ideal for companies with a global business model and whose employees are scattered around the world.

## Course Contents

1. Semiconductor Fundamentals
   - Resistance, Voltage, Current, Capacitance
   - The electric circuit, Ohm's Law
   - The PN junction
   - The Integrated Circuit
   - Digital versus Analog circuits

2. The Microchip
   - What is an Integrated Circuit?
   - The advantages of ICs and their Applications
   - Wafer fabrication technology
   - Memory versus Logic microchips
   - FLASH memory, DRAM memory
   - The MOSFET transistor - how does it work?
   - CMOS technology & power consumption
   - What is a technology node?
   - Strained silicon, Hi-k dielectrics
   - Multiple core microchips

3. Overview of Microchip Design
   - The microchip family tree; Digital, Analog, Memory RF, MEMs, Power ICs
   - Design considerations: application definition, operating frequency, I/O count, power requirements
   - Microchip design tools: EDA, ESL
   - Digital Logic, RTL generation, Statistical Process Variation, Mask generation, silicon prototype and debug
   - Microchip reliability

4. Overview of Silicon Process Technology
   - Cleaning technology and clean rooms
   - Photolithography, immersion and EUV lithography
   - Microelectronic etch, principles and equipment
   - Atomic Layer Deposition (ALD), concept and applications
   - Epitaxial deposition, function and application
   - Chemical and Mechanical Polishing (CMP); purpose, applications and equipment
   - Chemical Vapor Deposition (CVD); the purpose of depositing thin films and the equipment used
   - Electroplating Copper for Dual Damascene structures
   - Physical Vapor Deposition (PVD); depositing metal films
   - Ion Implantation: changing the electrical behavior of Silicon
   - Rapid Thermal Processing (RTP); annealing to remove implant damage

5. Overview of Microchip Processing
   - DIBL - the problem with planar transistors
   - The microchip fabrication hierarchy
   - Planar transistors versus FinFETs
   - FinFETS versus Nanosheets
   - The FinFET manufacturing process:
     - Well definition, Self-Aligned Double Patterning
     - Fin formation and Shallow Trench Isolation
     - Gate formation
     - Strained Silicon fabrication
     - Back-End metallization

6. Overview of Microchip Packaging
   - The microchip packaging hierarchy
   - Separating the microchips from the wafer
   - Wire bonding versus solder bumping versus Copper pillars
   - The many types of microchip packages:
     - Multi-chip modules, System in Package (SiP), System on Chip (SoC), Package-on Package (PoP), Package-in-Package (PiP), System in Package (SiP)
     - Fan-Out Wafer Level Packaging
   - 3D packaging: the concept, the promise and the problems

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**COURSE DATES:** **A 1.5-DAY ONLINE COURSE**

**AMERICA:** OCTOBER 11, 12 **EUROPE:** OCTOBER 18, 19 **ASIA:** OCTOBER 25, 26

## How Online Learning Works:

Shortly after registration you will be emailed a link that will take you to the online classroom on the day of the course. The week before the class begins a binder of color course notes will be shipped to you via Fedex or UPS.

The class is one-and-a half days long. On the day of the class you simply click on the link that has been provided and you will be seamlessly taken to the online classroom where you will be able to see, hear and interact with the instructor.

## Who Should Attend:

- New hires
- Purchasing and marketing personnel
- Patent Attorneys
- Product Engineers
- Sales and Application Engineers
- Materials Suppliers & Applications Engineers
- Anyone who is interested in learning the basics of microchip technology

## Tuition: $995

## Course Instructor:

The best instructor in the business teaches this course. Unlike other introductory courses that are taught by amateurs with no experience in making microchips, Jerry Healey is world-class expert in the field, with decades of industry experience. However, he is renown not just for his deep technical expertise, but also for his ability to present complex technical information in a clear and engaging manner. Mr. Healey is a talented public speaker, and the course notes for this seminar are profusely illustrated with high-quality 3D color graphics and relevant SEMs and TEMs. We want you to leave this course with a clear understanding of the key enabling technologies that have made the 5nm node microchip technology a reality, as well as an understanding of what the central technical challenges are for the 3nm node and beyond. After you have completed this course you will never again leave a meeting wondering what people were talking about.

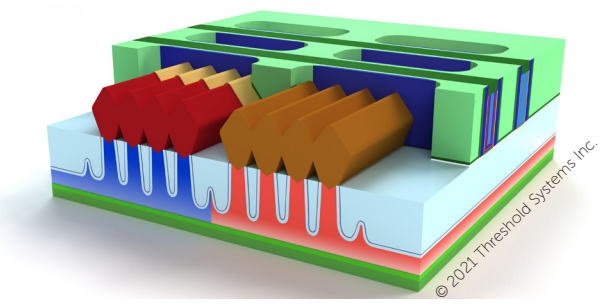
**Jerry Healey** has been a technical professional in the semiconductor industry for 30 years, 8 years of which were spent as a Device Engineer at Motorola Semiconductor. He was formerly an instructor for UC Berkeley Extension (College of Engineering), and was also employed as a Process Integration Engineer at both Sematech and the Advanced Technology Development Facility (ATDF), where he worked on advanced technology node development.

He is a renowned lecturer in the field of silicon processing, and his areas of expertise include process integration, technology transfer of new processes from R&D into manufacturing, and Nanosheet and FinFET fabrication. His audiences remember him for the breadth of his knowledge regarding semiconductor manufacturing, his engaging lecture style, and the insightful color graphics he uses to illustrate his lectures.

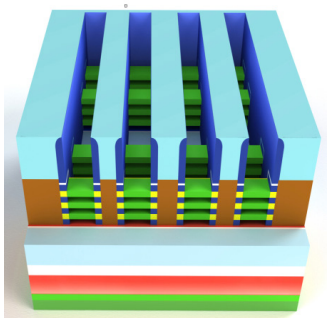
## Course Graphics:

This course is renown for the high-quality color graphics that are used throughout the 200+ pages of the course notes. Each graphic is carefully selected to illustrate specific points regarding the technology being discussed. Many of the graphics are original 3D illustrations that clearly convey key technical points regarding microchip technology.

**FinFET Transistors**




**Nanosheet Transistors**





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